

Description

[OVERLAY MARK AND METHOD OF FABRICATING THE SAME]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92127630, filed October 6, 2003.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The invention relates to an overlay mark and a method of fabricating the same, capable of solving the problem of alignment measurement caused by low step height of the outer mark.

[0004] Description of the Related Art

[0005] In addition to the control of critical dimension (CD), factors for a successful photolithography process on a wafer include alignment accuracy (AA). Therefore, the measurement of accuracy, that is, the measurement of overlay error is crucial to the semiconductor fabrication process. An

overlay mark is used as a tool for measuring overlay error and to determine whether the photoresist pattern is precisely aligned with the previous wafer layer on a wafer after a photolithography process.

- [0006] Conventionally, the overlay marks are located on the corners of the edge of each chip to measure whether the photoresist pattern is aligned with the previous wafer layer in the fabrication process.
- [0007] Figures 1A to 1C are cross sectional views illustrating a method of fabricating a metal interconnect having a via (via 0) and an overlay mark. Referring to Figure 1, a substrate 100 is provided, wherein the substrate 100 includes a chip region 102 and an overlay mark region 104. The dielectric layer 106a is formed on the substrate 100, and then the dielectric layer 106a is patterned to form a contact hole 108 in the dielectric layer 106a on the chip region 102. The subsequent process is another contact formation step, rather than a wire line forming step, so that no overlay mark is formed in the dielectric layer 106a on the overlay mark region 104.
- [0008] As shown in Figure 1A, the contact hole 108 is filled with tungsten 107a, and then a dielectric layer 110a is formed on the dielectric layer 106a. Thereafter, the dielectric layer

110a is patterned to form a via hole (via 0) in the dielectric layer 110a on the chip region 102 and a trench 114 in the dielectric layer 110a on the overlay mark region 104 simultaneously, wherein the trench 114 serves as a outer mark. Subsequently, a tungsten layer 116 is formed on the dielectric layer 110a to fill into the via hole and trench 114.

- [0009] Referring to Figure 1B, a chemical mechanical polishing process is performed on the tungsten layer 116 (in FIG. 1A) until the dielectric layer 110a is exposed to form a via (via 0) 112 on the chip region 102 and leave tungsten layer 116a in the trench 114 on the overlay mark region 104.
- [0010] Referring to Figure 1C, a metal layer 118 is formed on the substrate 100 for forming wire lines. A patterned photoresist layer 120 is formed on the metal layer 118. The portion of the patterned photoresist layer 120 on the chip region 102 serves as a mask for defining wire lines, and the other portion of the patterned photoresist layer 120a on the overlay mark region 104 serves as inner mark.
- [0011] In general, the dielectric layer 110a used for forming via hole (via 0) is thinner than the dielectric layer 106a, so that the trench 114 is mostly filled with the metal layer

116a after performing the chemical mechanic polishing process. Therefore, when the overlay mark is used to measure the alignment accuracy, the peak signal t of the outer mark can not be read because of low step height on the outer mark. Consequently, the overlay error can not be calculated.

SUMMARY OF INVENTION

- [0012] The invention provides an overlay mark and a method of fabricating the same to solve the problem of alignment measurement caused by low step height of the outer mark.
- [0013] The invention provides a method of fabricating an overlay mark. A first material layer is formed on a substrate, and then a first trench serving as a trench type outer mark is formed in the first material layer. Thereafter, a first deposition layer is formed on the first material layer, wherein the first trench is partially or incompletely filled with the first deposition layer. Subsequently, a first chemical mechanical polishing process is performed on the first deposition layer until the first material layer is exposed leaving the remaining first deposition layer in the first trench. A second material layer is formed to cover the first material layer and the first deposition layer. A portion of the sec-

ond material layer on the trench type outer mark is removed to form a second trench, wherein the second trench exposes at least a portion of the first deposition layer in the first trench. A second deposition layer is formed on the substrate, and then a second chemical mechanical polishing process is performed on the second deposition layer until the first material layer is exposed leaving the remaining portion of the second deposition layer in the second trench. A third deposition layer is formed on the second material layer and the second deposition layer. The first trench is partially or incompletely filled with the first deposition layer, so that a step height is formed on the third deposition between the edge of the first trench and the center of the first trench. A raised feature serving as an inner mark is formed on the third deposition layer.

[0014] The invention further provides a method of fabricating an overlay mark. A first material layer is formed on a substrate, and the first material layer is patterned to form a first raised feature serving as a portion of a raised type outer mark on the substrate. Subsequently, a first deposition layer is formed to cover the substrate and the first raised feature, and then a first chemical mechanical pol-

ishing process is performed on the first deposition layer until the top surface of the first raised feature is exposed. Thereafter, a second material layer is formed to cover the first deposition layer and the first raised feature, wherein a thickness of the second material layer is smaller than that of the first material layer. The second material layer is patterned to form a second raised feature serving as the other portion of the raised type outer mark on the first raised feature. Afterwards, a second deposition layer is formed to cover the first deposition layer, the second raised feature and the first deposition layer. The second deposition layer is thinner than the second feature. Subsequently, a second chemical mechanical polishing process is performed on the second deposition layer until the top surface of the second raised feature is exposed.

Thereafter, a third deposition layer is formed on the second material layer. A step height is formed on the third deposition layer between the edge of the second raised feature and the center of the second raised feature. Subsequently, the third raised feature serving as an inner mark layer is formed on the third deposition layer.

[0015] The invention further provides an overlay mark. The overlay mark comprises a first material, a first deposition

layer, a second material layer, a second deposition layer, a third deposition layer and a raised feature. The first material layer having a first trench therein serves as a portion of a trench type outer mark. The first trench is partially or incompletely filled with the first deposition layer. The second material layer having a second trench therein serving as the other portion of the trench type outer mark, wherein a thickness of the second material layer is smaller than that of the first material layer and the second trench exposes at least a portion of the first deposition layer in the first trench. The second trench is partially or incompletely filled with the second deposition layer. The third deposition layer covers the second material and the second deposition layer. A step height is formed between the third deposition layer on the edge of the first trench and the third deposition layer on the center of the first trench, because the first trench and the second trench are partially or incompletely filled with the first deposition layer and the second deposition, respectively. The raised feature made of a patterned photoresist layer located on the third deposition layer to serves as an inner mark.

[0016] The invention further provides an overlay mark. The overlay mark comprises a first raised feature, a first deposition

layer, a second raised feature, a second deposition layer, a third deposition layer and a third raised feature. The first raised feature serving as a portion of a raised type outer mark is on a substrate. The first deposition layer covers a side wall of the first raised feature and the substrate. The top surface of the first deposition layer on the substrate is lower than that of the first raised feature. The second raised feature serving as the other portion of the raised type outer mark covers the first raised feature, wherein a thickness of the second raised feature is smaller than that of the first raised feature. The second deposition layer covers a side wall of the first feature and the first deposition layer. The third deposition layer covers the second raised feature and the second deposition layer. A step height is formed on the third deposition layer between the edge of the second raised feature and the center of the second raised feature. The third raised feature made of a patterned photoresist layer is on the third deposition layer and serves as an inner mark.

- [0017] Since the outer mark has enough step height, the peak signal of the outer mark can be read. Therefore, the overlay error can be calculated.
- [0018] It is to be understood that both the foregoing general de-

scription and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

- [0019] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.
- [0020] Figures 1A to 1C are cross sectional views illustrating a method of fabricating a metal interconnect having a via (via 0) and an overlay mark according to the prior art.
- [0021] Figures 2A to 2J are cross sectional views illustrating a method of fabricating an overlay mark in a metal interconnect according to the first embodiment of this invention.
- [0022] Figures 3A to 3D are cross sectional views illustrating a method of fabricating an overlay mark in a metal interconnect according to the second example of the first embodiment of this invention.
- [0023] Figures 4A to 4I are cross sectional views illustrating a method of fabricating an overlay mark in a metal inter-

connect according to the second embodiment of this invention.

[0024] Figures 5A to 5D are cross sectional views illustrating a method of fabricating an overlay mark in a metal interconnect according to the second example of the second embodiment of this invention.

DETAILED DESCRIPTION

[0025] In the overlay mark of this invention and the method of fabricating the same, the step height of the outer mark is increased, so that the peak signal of the outer mark can be read. Therefore, the overlay error can be calculated. The following detail description relating to the method of fabricating an overlay mark in a metal interconnect process are exemplary and explanatory only and are not restrictive of the invention. Other embodiments of this invention will appear to those skilled in the art from consideration of the specification and practice of the invention disclosed herein.

[0026] Figures 2A to 2J are cross sectional views illustrating a method of fabricating an overlay mark in a metal interconnect according to the first embodiment of this invention, which only show the overlay mark region in the wafer similar to the overlay mark region 104 in Figures 1A to

1C.

[0027] Referring to Figure 2A, in the metal interconnect process, a dielectric layer 106 is first formed on the substrate 100. Referring to Figure 2B, a photolithographic process and an etching process for patterning the dielectric layer 106 are conducted to form a patterned dielectric layer 106a. The portion of patterned dielectric layer 106a on the chip region of the substrate 100 has a contact hole therein (not shown), and the portion of the patterned dielectric layer 106a on the overlay mark region 104 has a trench 200 therein. The trench 200 serves as a portion of an outer mark. In an embodiment, the trench 200 consists of four trenches, and the four trenches enclose a rectangle, and the width of the trench 200 is larger than that of the contact hole on the chip region.

[0028] Referring to Figure 2C, a metal layer 107 such as a tungsten layer is formed on the patterned dielectric layer 106a to fill in the contact hole and the trench 200. In general, the metal layer 107 is thinner than that of the dielectric layer 106a. Because the width of the trench 200 is larger than that of the contact hole, the trench 200 is partially or incompletely filled with the metal layer 107 when the contact hole is filled with the metal layer. In other words, a

step height is formed on the metal layer 107 between the edge of the trench 200 and the center of the trench 200.

- [0029] Referring to Figure 2D, a chemical mechanical polishing process is performed on the metal layer 107 until the patterned dielectric layer 106a is exposed to form a contact plug (not shown) on the chip region and leave the remaining metal layer 107a in the trench 200. The metal layer 107a left in the trench 200 retains the step height.
- [0030] Thereafter, referring to Figure 2E, another dielectric layer 110 is formed on the patterned dielectric layer 106a, in which a via will be formed therein in the subsequently process. In general, the dielectric layer 110 is thinner than the dielectric layer 106a. The thickness of the dielectric layer 106a is, for example, about 8000 angstrom, and the thickness of the dielectric layer 110 is about 3000 angstrom.
- [0031] Referring to Figure 2F, a photolithographic process and an etching process for patterning the dielectric layer 110 are conducted to form a patterned dielectric layer 110a. The portion of patterned dielectric layer 110a on the chip region of the substrate 100 has a via hole therein (not shown). The portion of the patterned dielectric layer 110a on the overlay mark region 104 has a trench 210 therein,

wherein the trench 210 serves as the other portion of the outer mark. The width of the trench 210 is larger than that of the trench 200, and the trench 210 exposes the metal layer 107a in the trench 200 and a portion of the patterned dielectric layer 106a. The difference in distance 202 between a side wall of the trench 210 and that of the trench 200 is no less than 150 nm.

[0032] Subsequently, referring to Figure 2G, another metal layer 116 such as a tungsten layer is formed to cover the dielectric layer 110a and fill in the via hole on the chip region and fill in the trench 210 on the overlay mark region 104. When the thickness of the second metal layer 116 is similar to that of the second dielectric layer 110, the trench 210 is partially or incompletely filled with the metal layer 116, because the trench 200 is partially or incompletely filled with the metal layer 107. In other words, the step height is maintained in the metal layer 116 between the edge of the trench 200 and the center of the trench 200.

[0033] Referring to Figure 2H, a chemical mechanical polishing process to the metal layer 116 is performed until the patterned dielectric layer 110a is exposed to form a via plug (not shown) on the chip region and leave the metal layer

116a in the trench 210 on the overlay mark region 104. The metal layer 116a left in the trench 210 keeps the step height of the metal layer 107a when the thickness of the metal layer 116 is similar to that of the dielectric layer 110a.

- [0034] Referring to Figure 2I, a metal layer 118 used for forming wire lines connected to the via plug on the chip region is formed on the dielectric layer 110a. Referring to Figure 2J, a patterned photoresist layer 120 is formed on the metal layer 118. The portion of the patterned photoresist layer 120 on the chip region serves as a mask for defining wire lines, and the portion 120a of the patterned photoresist layer on the overlay mark region 104 serves as an inner mark.
- [0035] Again, referring to Figure 2J, the step height is formed on the metal layer 118 between the edge of the trench 200 and the center of the trench 200, because the trenches 200 and 210 are partially or incompletely filled with the first deposition layer and the second deposition, respectively. Using the overlay mark to measure the alignment accuracy, the peak signal in the center point of the outer mark, which is indicated by the dotted line 210, can be read, since the outer mark has a high step height. More-

over, the peak signal in the center point of the inner mark, which is indicated by the dotted line 212, can be read.

Thereafter, the overlay error can be determined. For example, the overlay error can be decided by the difference in distance A between the peak signal in the center point of the outer mark and the peak signal in the center point of the inner mark.

[0036] Another example of the first embodiment of the present invention is described as follows. Figure 3A is a cross sectional view illustrating a method of fabricating an overlay mark in a metal interconnect according to the first embodiment of this invention, which is a subsequent step following Figure 2E. Referring to Figure 3A, a photolithographic process and an etching process for patterning the dielectric layer 110 are conducted to form a patterned dielectric layer 110b. The portion of patterned dielectric layer 110b on the chip region of the substrate 100 has a via hole therein (not shown). The portion of the patterned dielectric layer 110b on the overlay mark region 104 has a trench 210a therein, the trench 210a serves as the other portion of the outer mark. The width of the trench 210a is smaller than that of the trench 200, and the trench 210a exposes a portion of the metal layer 107a in the trench

200.

[0037] Referring to Figure 3B, another metal layer 116 such as a tungsten layer is formed to cover the dielectric layer 110b and fill into the trench 210a. Thereafter, a chemical mechanical polishing process is performed on the metal layer 116 until the dielectric layer 110b adjacent the trench 200 is exposed. Thereby, a via plug (not shown) on the chip region is formed and the metal layer 116a over the metal layer 107a remain on the overlay mark region 104. The metal layer 116a retains the step height of the metal layer 107a when the thickness of the metal layer 116 is similar to that of the dielectric layer 110a.

[0038] Subsequently, referring to Figure 3D, a metal layer 118 used for forming wire lines connected to the via plug on the chip region is formed on the dielectric layer 110b. Thereafter, a patterned photoresist layer 120 is formed on the metal layer 118. The portion (not shown) of the patterned photoresist layer 120 on the chip region serves as a mask for defining wire lines, and the portion 120a of the patterned photoresist layer 120 on the overlay mark region 104 serves as an inner mark.

[0039] Referring to Figures 2J and 3D, the overlay mark of this embodiment comprises a dielectric layer 106a, a metal

layer 107a, a dielectric layer 110a or a dielectric layer 110b, a metal layer 116a, a metal layer 118 and a raised feature 120a. The dielectric layer 106a having a first trench 200 therein serves as a portion of the trench type outer mark. The first trench 200 is partially or incompletely filled with the metal layer 116a. A thickness of the dielectric layer 110a or 110b having a second trench 210 or 210a therein is smaller than that of the dielectric layer 106a. Therefore, the second trench 210 or 210a exposes at least a portion of the metal layer 107a in the first trench 200. The second trench 210 or 210a is partially or incompletely filled with the metal layer 116a, wherein the second trench 210 or 210a serves as the other portion of the trench type outer mark. The metal layer 118 covers the dielectric layer 110a or 110b and the metal layer 116a. A high step height is formed on the metal layer 118 between the edge of the first trench 200 and the center of the first trench 200, because the first trench 200 and the second trench 210 are partially or incompletely filled with the metal layer 107a and metal layer 116a, respectively. The raised feature 120a made of a patterned photoresist layer located on the metal layer 118 serves as an inner mark. Using the overlay mark to measure the alignment

accuracy, the peak signal in the center point of the outer mark, which is indicated by the dotted line 210, can be read, since the outer mark has a high step height. Moreover, the peak signal in the center point of the inner mark, which is indicated by the dotted line 212, can be read. Thereafter, the overlay error can be determined.

- [0040] In the first embodiment, the trench type outer mark is provided for forming the outer mark of the overly mark. On the other hand, a raised type outer mark is provided for forming the outer mark of the overly mark.
- [0041] Figures 4A to 4I are cross sectional views illustrating a method of fabricating an overlay mark in a metal interconnect according to the second embodiment of this invention. Referring to Figure 4A, in the metal interconnect process, a dielectric layer 106 is first formed on the substrate 100. Referring to Figure 4B, a photolithographic process and an etching process for patterning the dielectric layer 106 are conducted to form a patterned dielectric layer 106a. The portion of patterned dielectric layer 106a on the chip region of the substrate 100 has a contact hole therein (not shown), and the portion of the patterned dielectric layer on the overlay mark region 104 is a first raised feature 300. The first raised feature 300 serves as a

portion of an outer mark. In an embodiment, the first raised feature 300 consists of four protrusions, and the four protrusions enclose a rectangle (not shown).

[0042] Referring to Figure 4C, a metal layer 107 such as a tungsten layer is formed on the substrate 100 to fill in the contact hole on the chip region and to cover raised feature 300 on the overlay mark region 104. The thickness of the metal layer 107 is thinner than that of the raised feature 300. Thereafter, referring to Figure 4D, a chemical mechanical polishing process is performed on the metal layer 107 until the patterned dielectric layer 106a is exposed. Thereby, a contact plug (not shown) is formed on the chip region, and the metal layer 107a is remained on the side wall of the first raised feature 300 and covering the substrate 100 on the overlay mark region 104. The thickness of the metal layer 107 is thinner than that of the first raised feature 300. Therefore, on the overlay mark region 104, the top surface of the remained metal layer 107a on the substrate 100 is lower than the top surface of the first raised feature 300 after performing the chemical mechanical polishing process.

[0043] Referring to Figure 4E, another dielectric layer 110 is formed on the substrate 100, in which a via will be formed

therein in the subsequently process. In general, the dielectric layer 110 is thinner than the dielectric layer 106a. The thickness of the dielectric layer 106a, for example, is about 8000 angstrom, and the thickness of the dielectric layer 110 is about 3000 angstrom.

[0044] Referring to Figure 4F, a photolithographic process and an etching process for patterning the dielectric layer 110 are conducted to form a patterned dielectric layer 110c. The portion of patterned dielectric layer 110c on the chip region of the substrate 100 has a via hole therein (not shown). The portion of the patterned dielectric layer 110c on the overlay mark region 104 is a second raised feature 310, which serves as the other portion of the outer mark. The first raised feature 300 and the second raised feature 310 compose the outer mark 320. A width of the second raised feature 310 is smaller than that of the first raised feature 300, and so that the second raised feature 310 exposes a portion of the first raised feature 300. The difference in distance 302 between a side wall of the first raised feature 300 and that of the second raised feature 310 is no less than 150 nm.

[0045] Subsequently, referring to Figure 4G, another metal layer 116 such as a tungsten layer is formed to cover the sec-

ond raised feature 310, the first feature 300 and the metal layer 107a on the overly mark region 104, and to cover the dielectric layer 110c and fill in the via hole on the chip region. In general, the thickness of the metal layer 116 is similar to that of the second raised feature 310. Therefore, on the overlay mark region 104, the top surface of the metal layer 116 on the second raised feature 310 is higher than that of the metal layer 116 on the metal layer 107a.

[0046] Referring to Figure 4H, a chemical mechanical polishing process is performed on the metal layer 116 until the patterned dielectric layer 110c is exposed. Thereby, a via plug (not shown) is formed on the chip region and the metal layer 116a is retained on the side wall of the second raised feature 310 and covering the metal layer 107a on the overlay mark region 104. On the overlay mark region 104, the top surface of the remained metal layer 116a on the metal layer 107a is lower than the top surface of the second raised feature 310 after performing the chemical mechanical polishing process. In other words, a high step height is formed between the top surface of the remained metal layer 116a on the metal layer 107a and the top surface of the second raised feature 310.

[0047] Referring to Figure 4I, a metal layer 118 used for forming wire lines connected to the via plug on the chip region is formed on the substrate 100. Thereafter, a patterned photoresist layer 120 is formed on the metal layer 118. The portion (not shown) of the patterned photoresist layer 120 on the chip region serves as a mask for defining wire lines, and the portion of the patterned photoresist layer 120 on the overlay mark region 104 serves as an inner mark 350.

[0048] Another example of the second embodiment of invention is described as follows. Figure 5A is a cross sectional view illustrating a method of fabricating an overlay mark in a metal interconnect according to the second embodiment of this invention, which is a subsequent step following Figure 4E. Referring to Figure 5A, a photolithographic process and an etching process for patterning the dielectric layer 110 are conducted to form a patterned dielectric layer 110d. The portion of patterned dielectric layer 110d on the chip region of the substrate 100 has a via hole therein (not shown). The portion of the patterned dielectric layer 110d on the overlay mark region 104 is a second raised feature 400, which serves as the other portion of the outer mark. The first raised feature 300 and the sec-

ond raised feature 400 constitute the outer mark 420. A width of the second raised feature 400 is larger than that of the first raised feature 300, and so that the second raised feature 400 covers the first raised feature 300 and the metal layer 107a adjacent to the second raised feature 400.

[0049] Referring to Figure 5B, another metal layer 116 such as a tungsten layer is formed to cover the second raised feature 310 and the metal layer 107a on the overly mark region 104, and cover the dielectric layer 110d and fill in the via hole on the chip region. The thickness of the metal layer 116 is similar to that of the second raised feature 310. Therefore, on the overlay mark region 104, the top surface of the metal layer 116 on the second raised feature 400 is higher than that of the substrate 100.

[0050] Referring to Figure 5C, a chemical mechanical polishing process is performed on the metal layer 116 until the patterned dielectric layer 110d is exposed. Thereby, a via plug (not shown) is formed on the chip region and the metal layer 116a is retained on the side wall of the second raised feature 400 and covering the metal layer 107a on the overlay mark region 104. On the overlay mark region 104, the top surface of the remained metal layer 116a on

the metal layer 107a is lower than the top surface of the second raised feature 400 after performing the chemical mechanical polishing process. In other words, a step height is formed between the top surface of the remained metal layer 116a on the metal layer 107a and the top surface of the second raised feature 400 on the overlay mark region 104.

- [0051] Referring to Figure 5D, a metal layer 118 used for forming wire lines connected to the via plug on the chip region is formed on the patterned dielectric layer 110d. Thereafter, a patterned photoresist layer 120 is formed on the metal layer 118. The portion (not shown) of the patterned photoresist layer 120 on the chip region serves as a mask for defining wire lines, and the portion of the patterned photoresist layer 120 on the overlay mark region 104 serves as an inner mark 350.
- [0052] Referring to Figures 4I and 5D, the overlay mark of this embodiment comprises a first raised feature 300, a metal layer 107a, a second raised feature 310 or 400, a metal layer 116a, a metal layer 118 and a third raised feature 350. The first raised feature 300 serves as a raised type outer mark on a substrate 100. The metal layer 107a covers a side wall of the first raised feature 300 and the sub-

strate100. The second raised feature 310 or 400 covers at least the first raised feature 300, wherein a thickness of the second raised feature 310 or 400 is smaller than that of the first raised feature 300. The metal layer 116a covers a side wall of the second feature 310 or 400 and the metal layer 107a. The metal layer 118 covers the second raised feature 310 or 400 and the metal layer 116a. The third raised feature 350 made of a patterned photoresist layer on the metal layer 118 serves as an inner mark. Using the overlay mark to measure the alignment accuracy, the peak signal in the center point of the outer mark, which is indicated by the dotted line 210, can be read, since the outer mark has a high step height. Moreover, the peak signal in the center point of the inner mark, which is indicated by the dotted line 212, can be read. Thereafter, the overlay error can be determined.

[0053] The above-mentioned process of fabricating overlay mark in the metal interconnect is illustrated according to preferred embodiments of the present invention, however, this is used as an example without restricting the scope of this invention. In other words, the dielectric layers 106 and 110 comprise other materials, for example, a conductive material or a silicon material. The metal layer 107,

116 and 108 comprise other material, for example, a dielectric material or a silicon material.

[0054] In this invention, the outer mark consists of two trenches or two raised features. The first trench or the first raised feature is formed by patterning the first dielectric layer for forming the contact hole. The second trench or the second raised feature is formed by patterning the second dielectric layer for forming the via hole (via 0). Since the metal layer for forming the contact plug is thinner than the first dielectric layer, a step height is formed between the remained metal layer and the dielectric layer for forming the contact hole after performing the chemical mechanical polishing process. Furthermore, the thickness of the second metal layer for forming the via 0 is similar to that of the second dielectric layer. Therefore, a high step height of the outer mark is kept after a second chemical mechanical polishing process and the problem of alignment measurement caused by low step height of the outer mark can be effectively resolved.

[0055] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is in-

tended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.